Amendments to the Specification:

Please replace paragraph 0005 with the following amended paragraph:

Referring ~~Please refer~~ to Fig.1. Fig.1 is a circuit diagram of a prior art differential pair circuit 10 used for transmitting data to a high speed serial bus. Serial data signal DATA is sent across the serial bus and transmitted by the differential pair circuit 10. The differential pair circuit 10 contains a first transistor M1 and a second transistor M2 for respectively producing a positive data signal DataP and a negative data signal DataN. In addition, a bias voltage Vbias is applied to a third transistor M3 for biasing the differential pair circuit 10. The first transistor M1 is controlled by a first control signal CTRL1 and the second transistor M2 is controlled by a second control signal CTRL2. Each of these control signals selectively opens and closes the corresponding transistors according to a value of the serial data signal DATA. The serial data signal DATA can either transmit a logical value of "0", "1" when in transmit mode, or not transmit any values when in idle mode. The following logic values are given under the assumption that first and second transistors M1 and M2 are PMOS transistors, although any kind of transistors could be used. Please see Table 1 below to see the relationship between values of the serial data signal DATA, the first and second control signals CTRL1 and CTRL2, and the positive and negative data signals DataP and DataN.

Please replace paragraph 0008 with the following amended paragraph:

A differential signal DIFF is calculated by subtracting the negative data signal DataN from the positive data signal DataP. Referring ~~Please refer~~ to Fig.2. Fig.2 is a timing diagram of the differential signal DIFF with respect to the serial data signal DATA. As shown in Fig.2, when the serial data signal DATA is in idle mode, the differential signal DIFF has a value of 0 volts since both the positive and negative data signals DataP and DataN have a value of 0 volts. When the serial data signal DATA is has a value of "1", the

differential signal DIFF has a value of +V volts (V represents a voltage value of logical "1") since the positive data signal DataP has a value of +V volts and the negative data signal DataN has a value of 0 volts. Finally, when the serial data signal DATA is has a value of "0", the differential signal DIFF has a value of -V volts since the positive data signal DataP has a value of 0 volts and the negative data signal DataN has a value of V volts. As shown by the sloped lines connecting the +V and –V values of the differential signal DIFF, low slew rates limit the speed at which the differential signal can change values.

Please replace paragraph 0009 with the following amended paragraph:

Unfortunately, when switching from idle mode to transmit mode, the prior art differential pair circuit 10 has a problem of non-uniform pulse widths. Referring ~~Please refer~~ to Fig.3. Fig.3 is a timing diagram showing pulse widths of data signals generated by the differential pair circuit 10. Values of the positive data signal DataP, the negative data signal DataN, and the differential signal DIFF are all shown with respect to time. From time t0 to t1, the serial data signal DATA is in idle mode. Therefore both the positive and negative data signals DataP and DataN and the differential signal DIFF all have a value of 0 volts. At time t1, the serial data signal data switches from idle mode to transmit mode, and the value of the positive data signal DataP begins to rise to +V volts. Because of the slew rate, however, it takes until time t2 to actually reach the value of +V volts. The value of positive data signal DataP continues to have a value of +V volts until time t4. At time t4, the value of the positive data signal DataP gradually begins to change to 0 volts, and by time t5, the value is back at +V volts. Finally, this value of +V volts is kept from time t5 until time t6. As shown from time t1 to t6, when in transmit mode, the negative data signal DataN has exactly the opposite logical value of the positive data signal DataP. Therefore, the differential signal DIFF ranges from a maximum value of +V volts to a minimum value of –V volts.

Please replace paragraph 0023 with the following amended paragraph:

Referring ~~Please refer~~ to Fig.4. Fig.4 is a circuit diagram of a pulse width control system 50 used in transmitting high speed serial data. The pulse width control system 50 functions much like the prior art differential pair circuit 10 shown in Fig.1.

Please replace paragraph 0026 with the following amended paragraph:

The first delay control cell 52 receives the first control signal CTRL1, delays the signal for a period of time, and then outputs a first delayed signal DEL1 to the first transistor M1. Likewise, the second delay control cell 54 receives the second control signal CTRL2, delays the signal for a period of time, and then outputs a second delayed signal DEL2 to the second transistor M2. Although all transistors shown in Fig.4 are shown as PMOS transistors, any type of transistors can be used in the present invention. Referring ~~Please refer~~ back to Table 1 to see the relationship between values of the serial data signal DATA, the first and second control signals CTRL1 and CTRL2, and the positive and negative data signals DataP and DataN.

Please replace paragraph 0028 with the following amended paragraph:

Referring ~~Please refer~~ to Fig.5. Fig.5 is a circuit diagram of a sample first delay control cell 52. The cell control signal CELL_CTRL is used to open and close a fourth transistor M4. Depending on the value of the cell control signal CELL_CTRL, the first control signal CTRL1 will either travel in parallel through the fourth transistor M4 and a resistor R, or travel only through the resistor R. The result will be the first delayed signal DEL1, which is simply a delayed version of the first control signal CTRL1. Specifically, if the cell control signal CELL_CTRL has a value of "0", the fourth transistor M4 will close.

This causes the first control signal CTRL to travel in parallel across the resistor R and the closed fourth transistor M4, which produces a short delay T1. On the other hand, if the cell control signal CELL_CTRL has a value of "1", the fourth transistor M4 will open. This causes the first control signal CTRL to travel solely across the resistor R, which produces a longer delay T2. The delay times T1 and T2 are chosen such that $T2 - T1 = \Delta T$. Remember that in the prior art differential pair circuit 10, ΔT is the amount of extra time contained in the first pulse after a switch from idle mode to transmit mode when compared to other pulses in transmit mode.

Please replace paragraph 0030 with the following amended paragraph:

Referring ~~Please refer~~ to Fig.6. Fig.6 is a timing diagram showing pulse widths of data signals generated by the pulse width control system 50. The dotted line pulses represent data signals that would have been generated with the prior art differential pair circuit 10. The solid line pulses represent data signals using the present invention pulse width control system 50. The solid line pulses are simply delayed versions of the dotted line pulses. From time t0 to time t1, the serial data signal DATA is in idle mode. Therefore both the positive and negative data signals DataP and DataN and the differential signal DIFF all have a value of 0 volts. At time t1, the serial data signal DATA switches from idle mode to transmit mode. At this time, the first control signal CTRL1 also changes to pass the value of the serial data signal DATA to the positive data signal DataP. However, since this is the first pulse after the transition from idle mode to transmit mode, the first delay control cell 52 delays the first control signal CTRL1 for a delay time T2. Thus the value of the positive data signal DataP begins to rise to +V volts at a time of t1 + T2. Because of the slew rate, however, it takes until time t2 to actually reach the value of +V volts. The value of the serial data signal DATA remains at +V volts until time t3, when it begins to fall back to 0 volts. At this time, the first control signal CTRL1 also changes to pass the value of the serial data signal DATA to the positive data signal DataP. First, since

this is not the first pulse in transmit mode, the first delay control cell 52 delays the first control signal CTRL1 for a delay time T1. Thus the value of the positive data signal DataP begins to fall to 0 volts at a time of t3 + T1, which is the same as time t4. Now in transmit mode, the first and second delay control cells 52 and 54 continue to delay the first and second control signals CTRL1 and CTRL2 for a delay time T1.